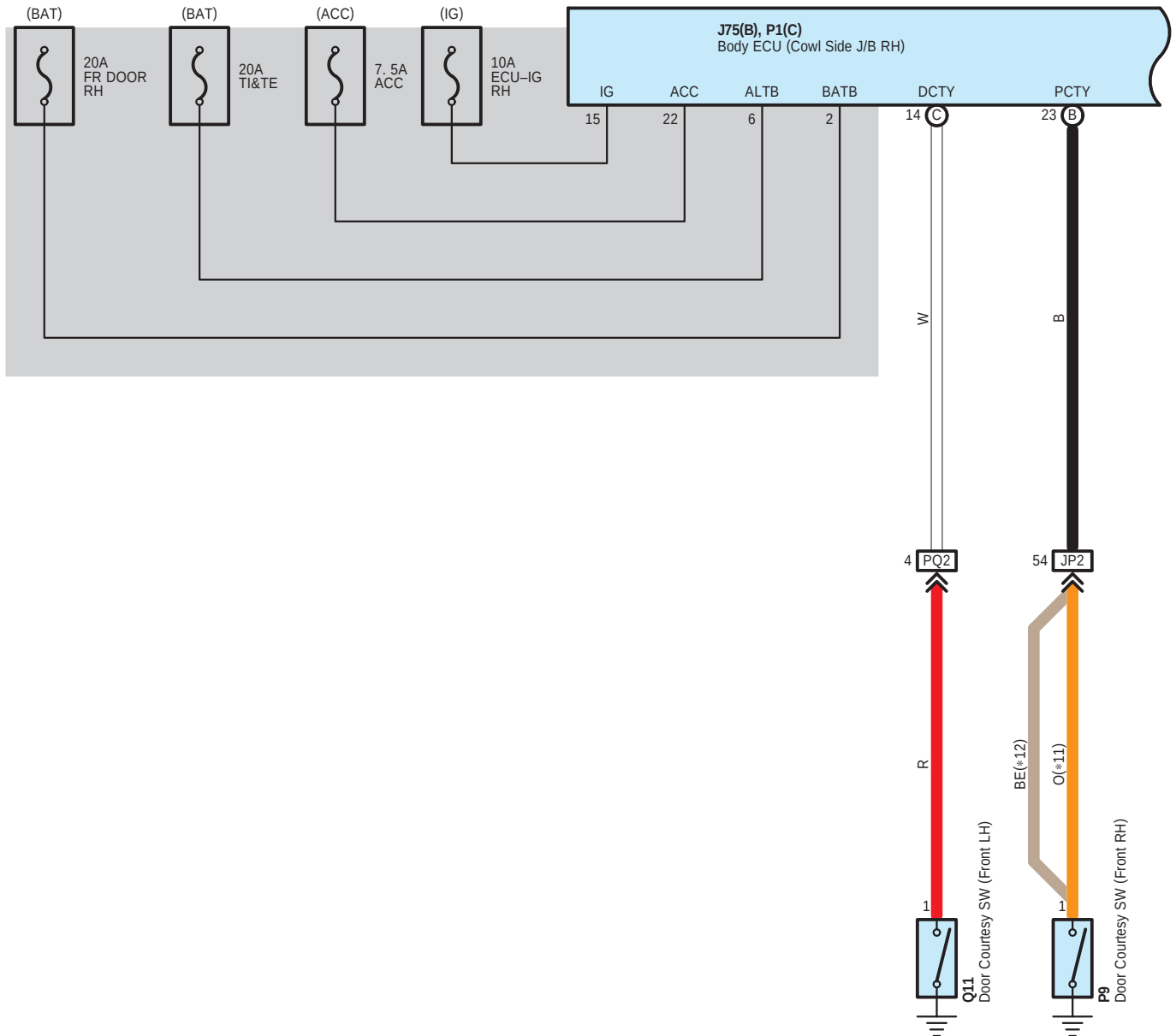
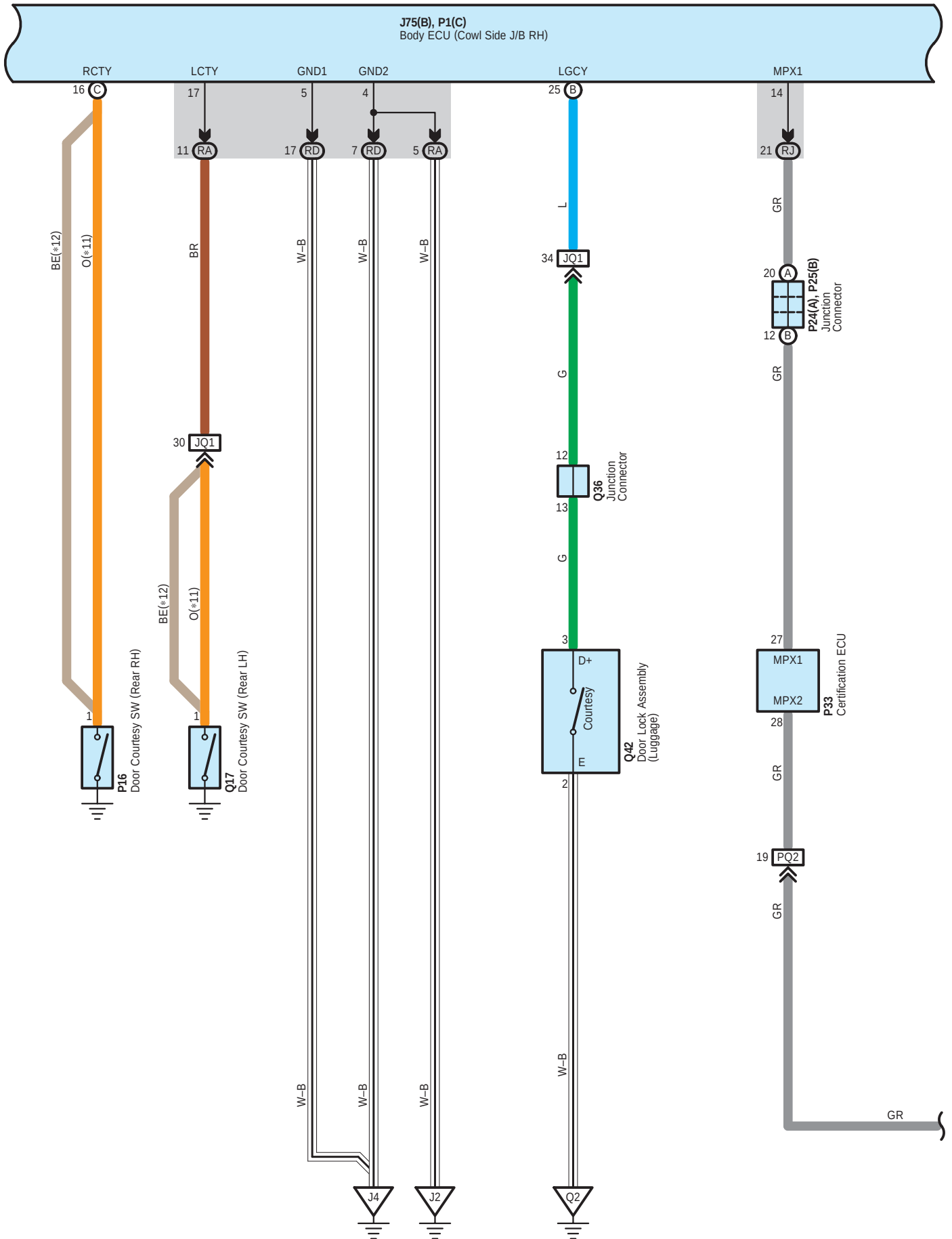


Door Lock Control <LHD>

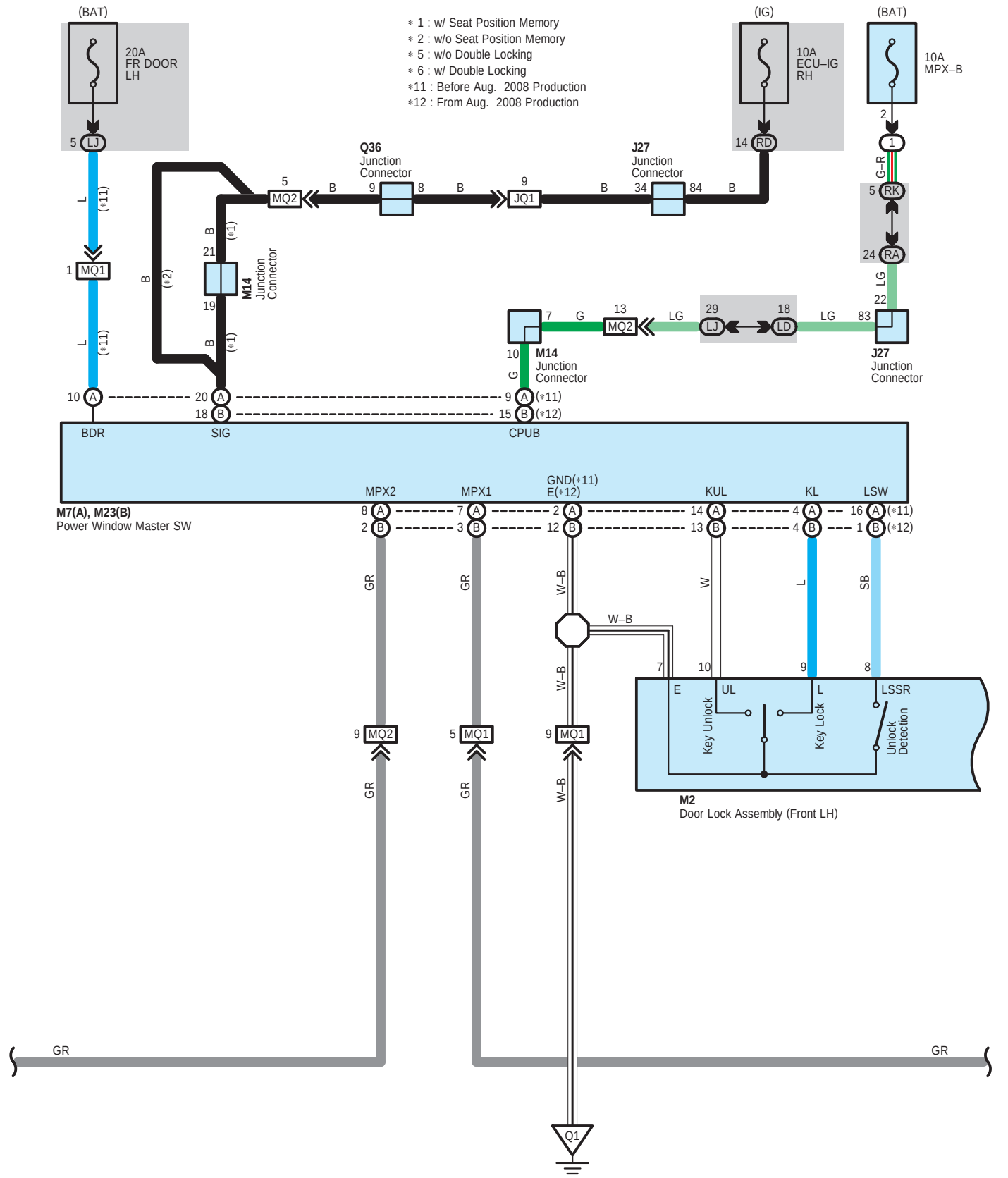


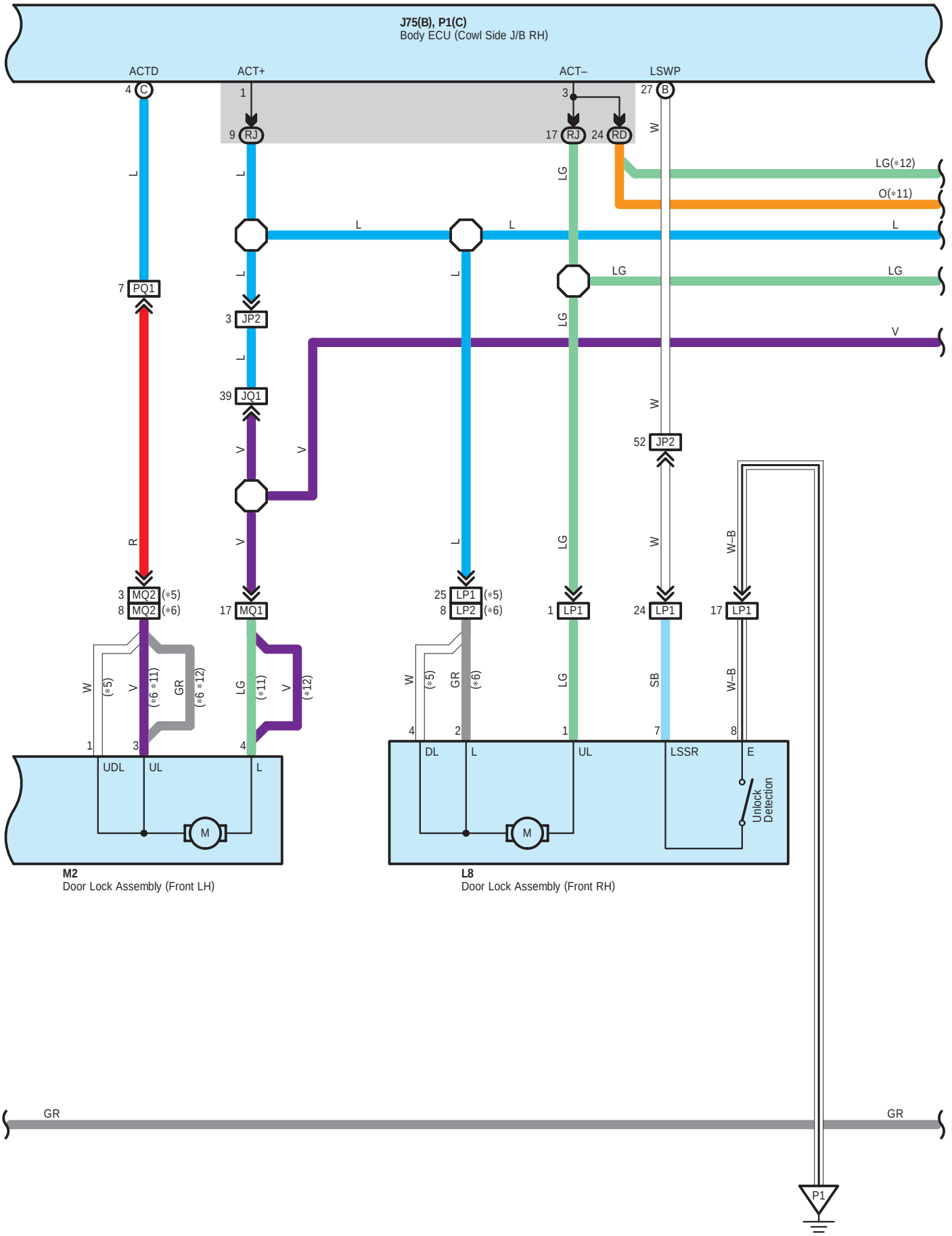
*11 : Before Aug. 2008 Production
 *12 : From Aug. 2008 Production

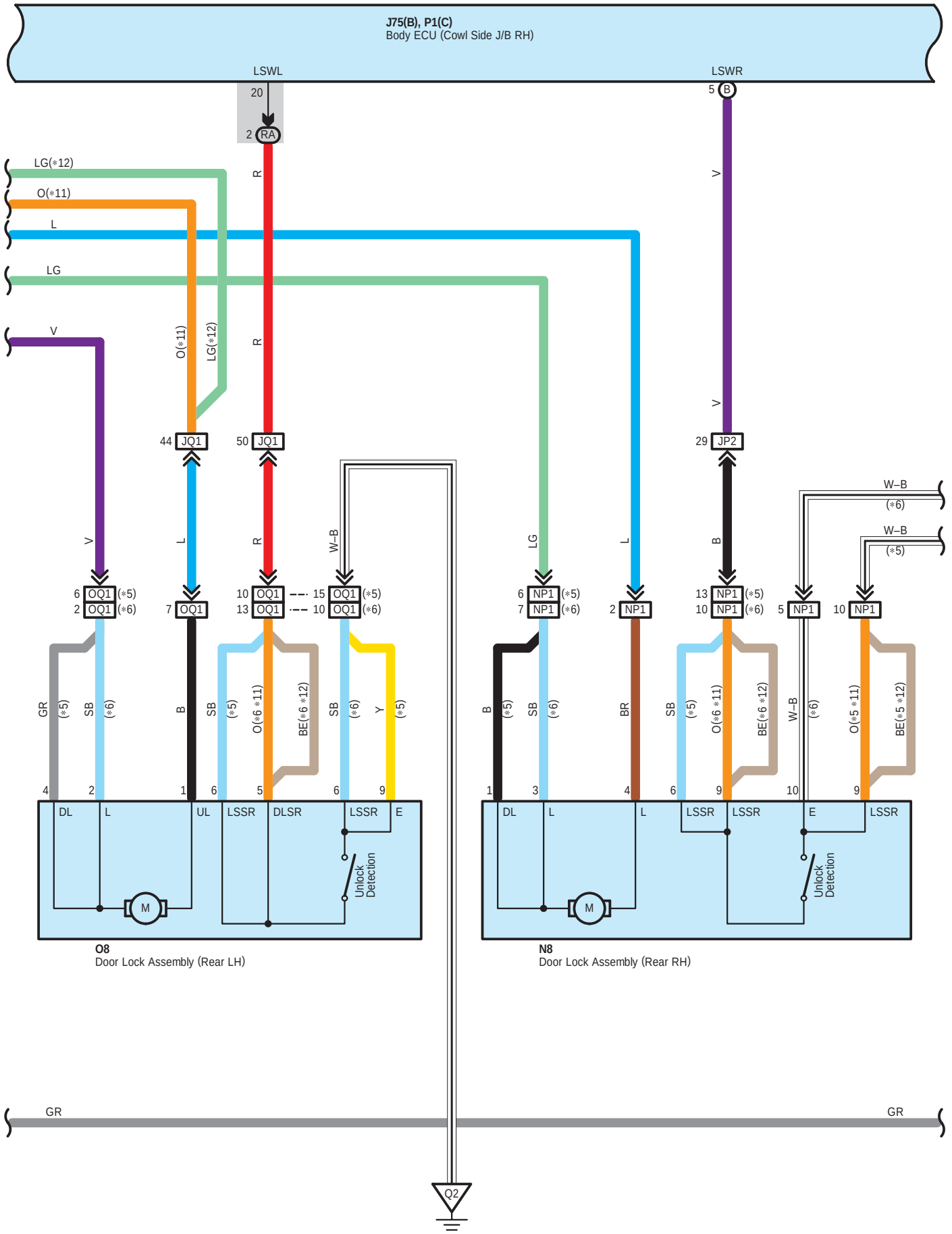
Door Lock Control <LHD>



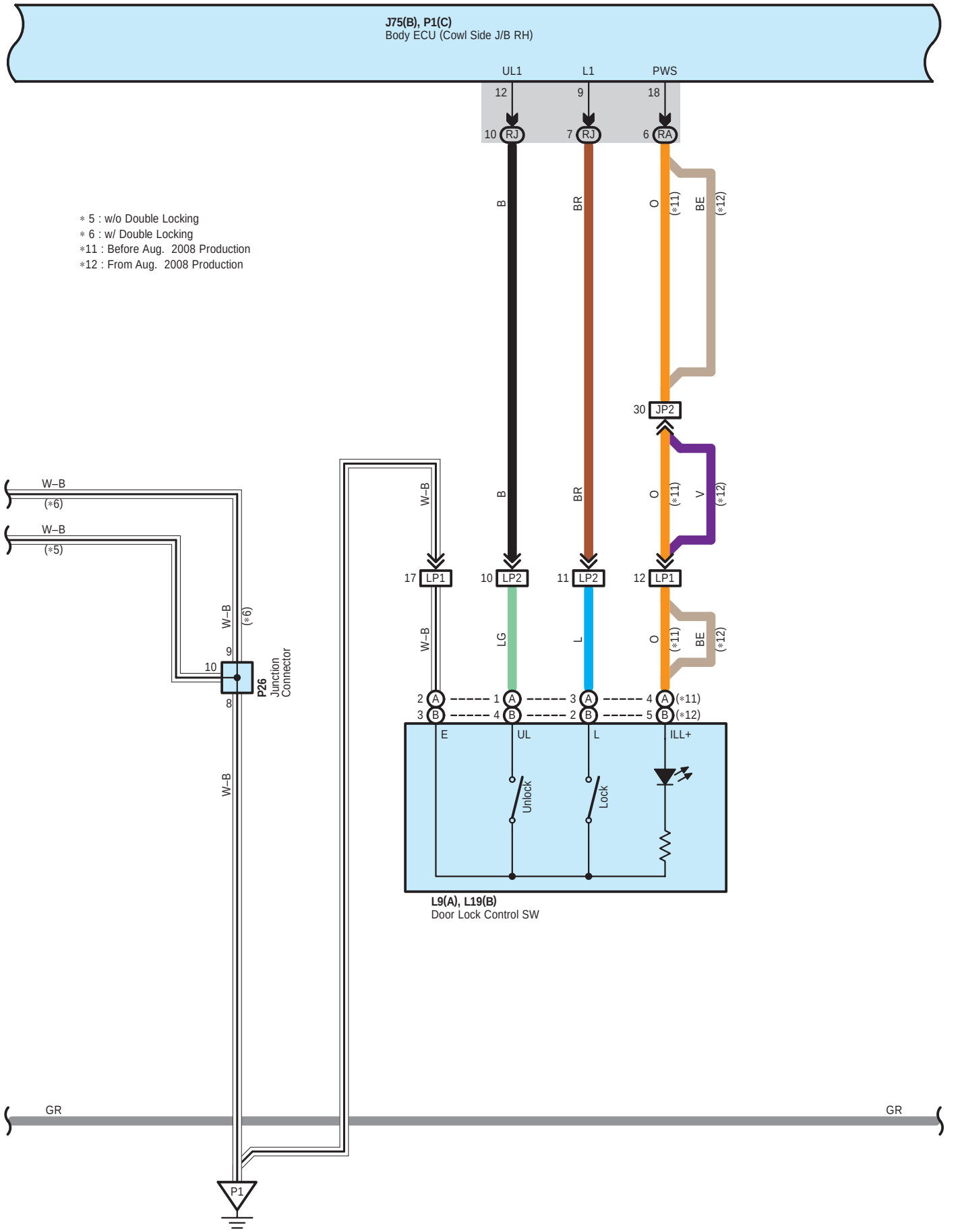
J75(B), P1(C)
Body ECU (Cowl Side J/B RH)

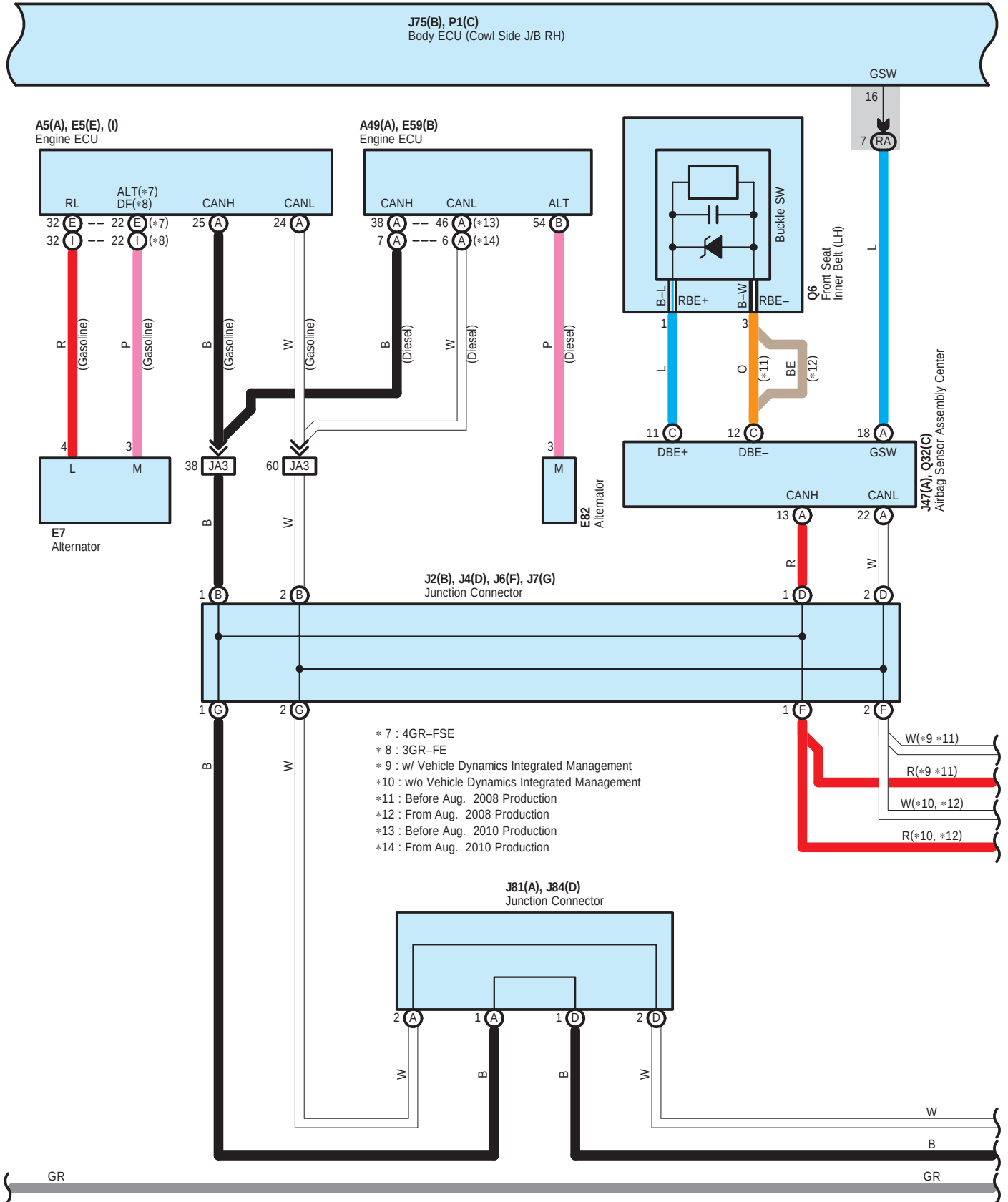






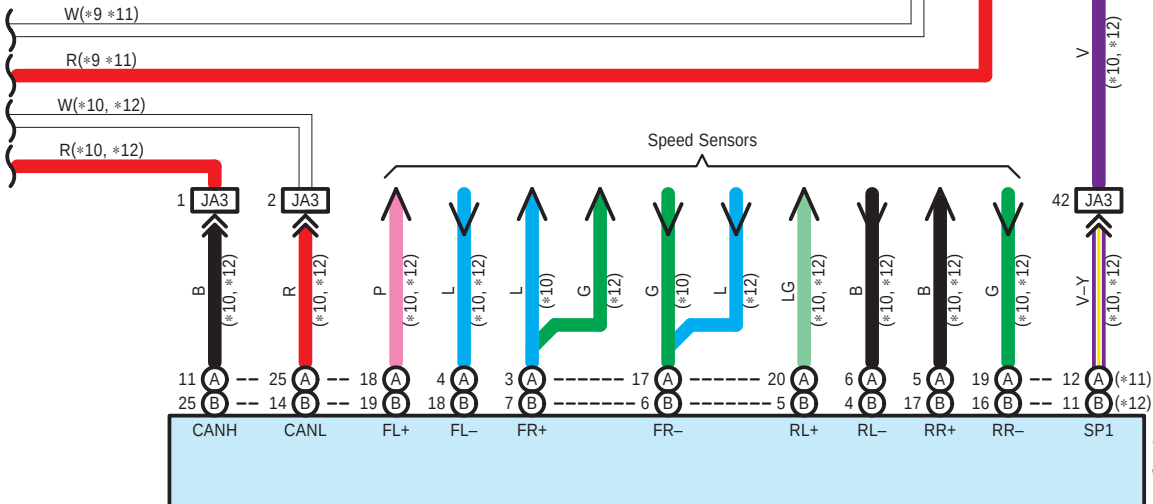
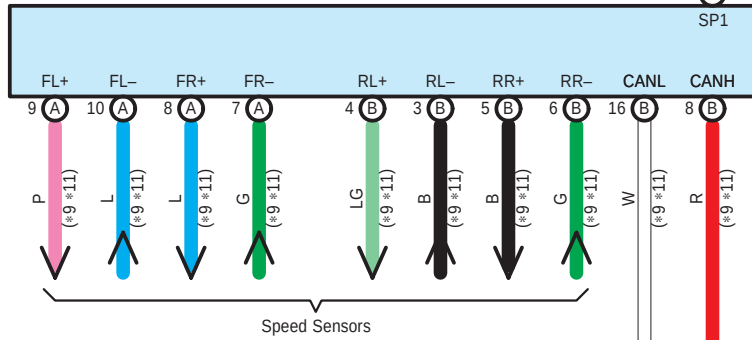
Door Lock Control <LHD>



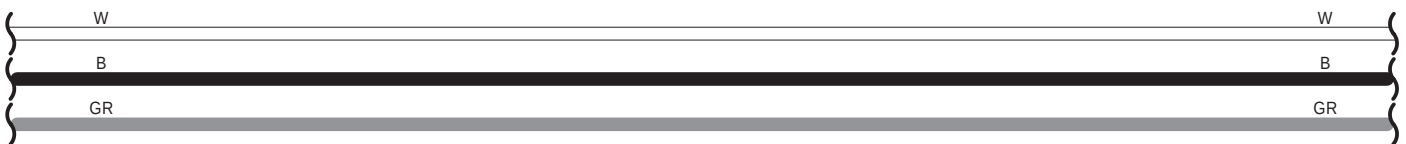


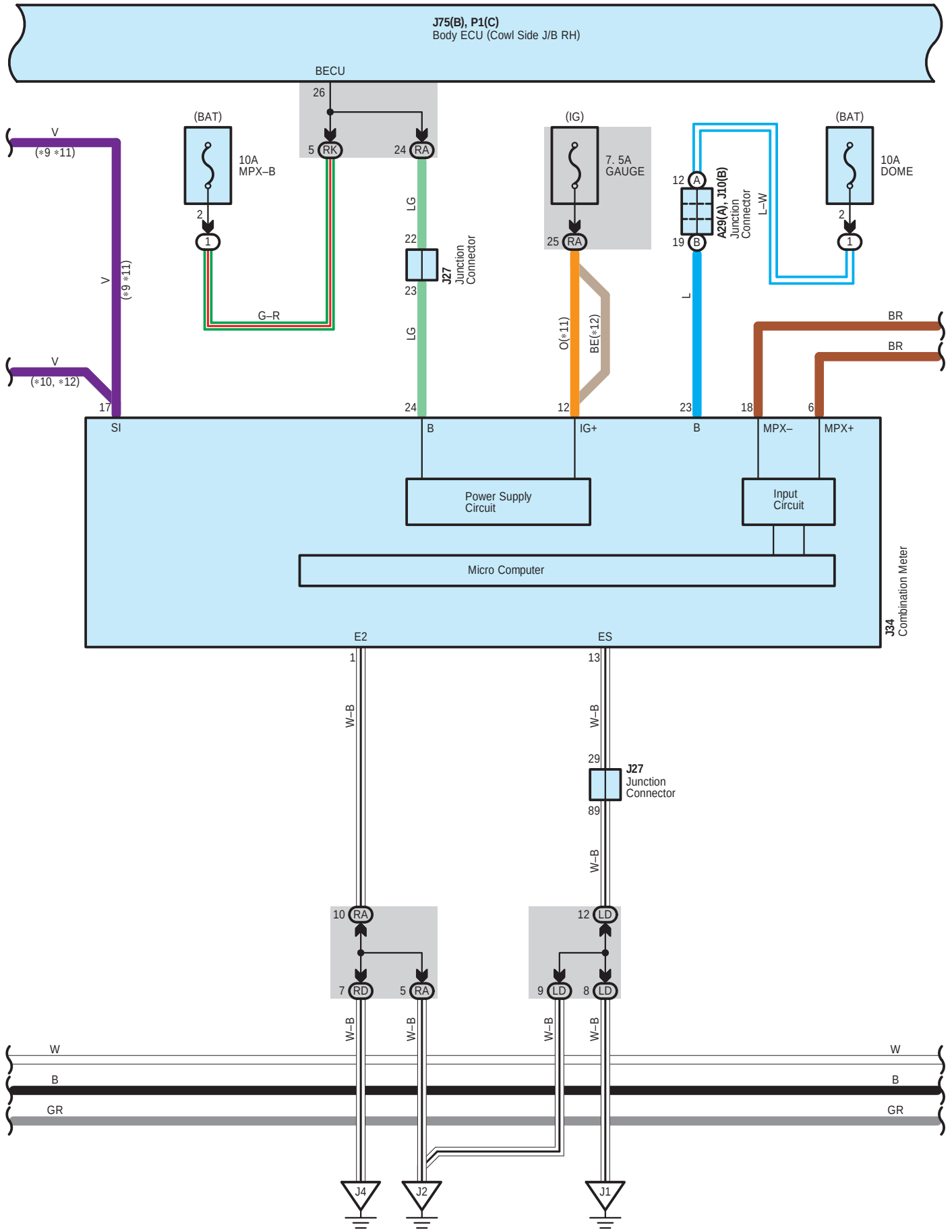
J75(B), P1(C)
Body ECU (Cowl Side J/B RH)

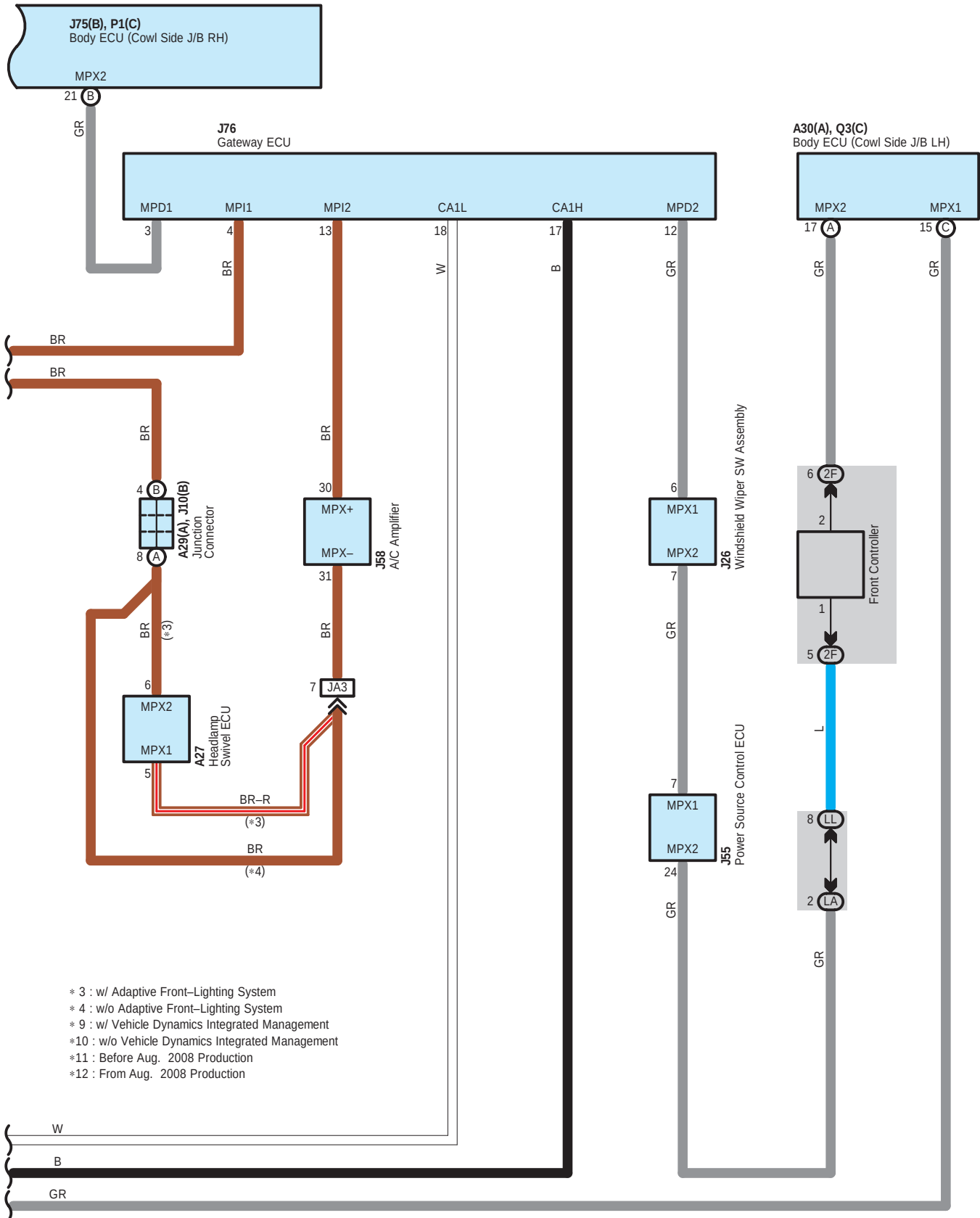
A35(A), J77(B)
Skid Control ECU



A14(A), A58(B)
Skid Control ECU
with Actuator

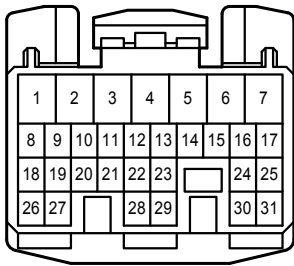




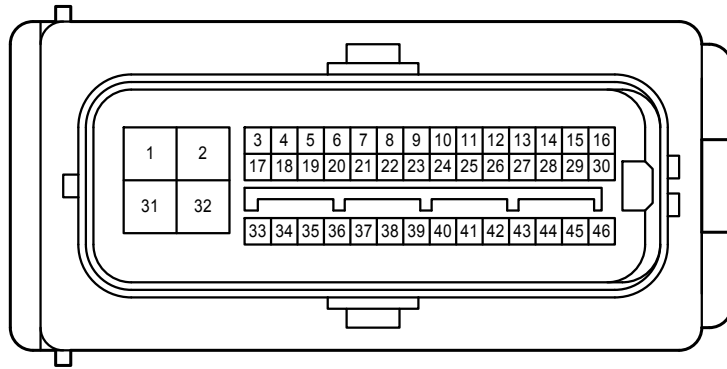


- * 3 : w/ Adaptive Front-Lighting System
- * 4 : w/o Adaptive Front-Lighting System
- * 9 : w/ Vehicle Dynamics Integrated Management
- * 10 : w/o Vehicle Dynamics Integrated Management
- * 11 : Before Aug. 2008 Production
- * 12 : From Aug. 2008 Production

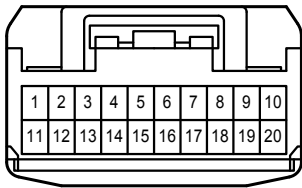
A 5
White



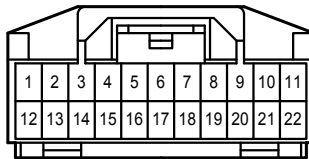
A 14
Black



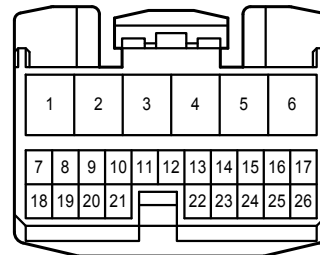
A 27
White



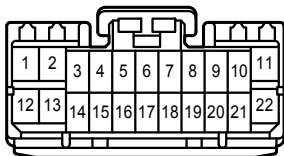
A 29
Blue



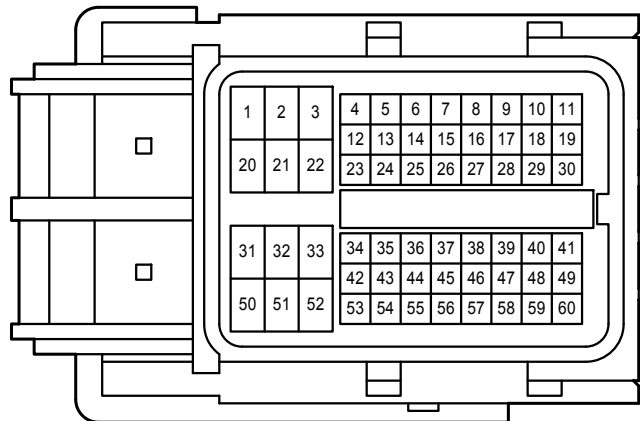
A 30
White



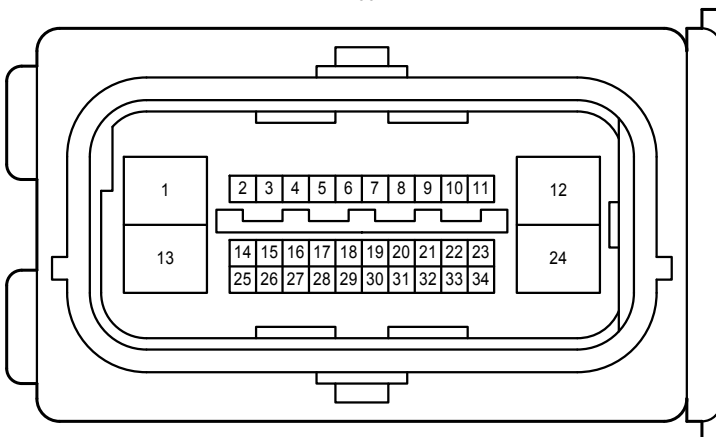
A 35
White



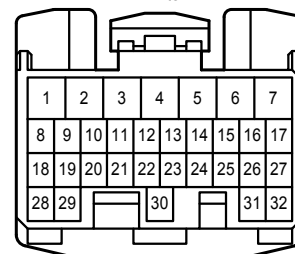
A 49
Black



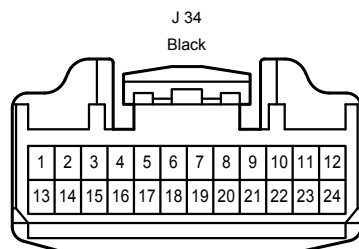
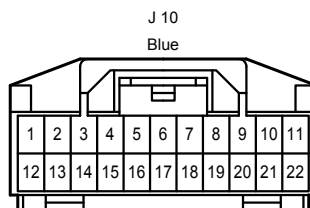
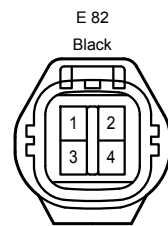
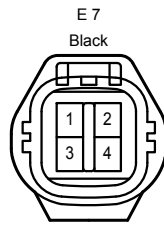
A 58
Black



E 5
White

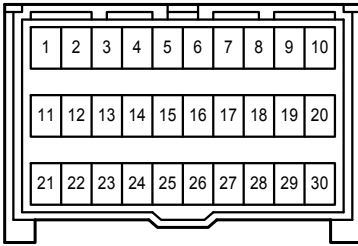


(4GR-FSE)

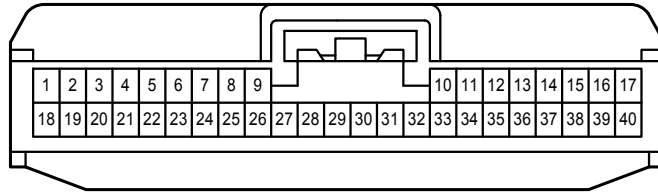


Door Lock Control <LHD>

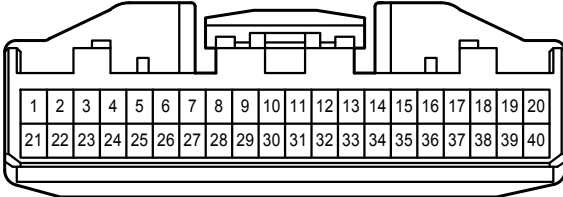
J 47
Yellow



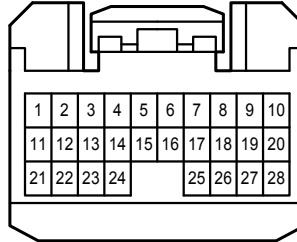
J 55
White



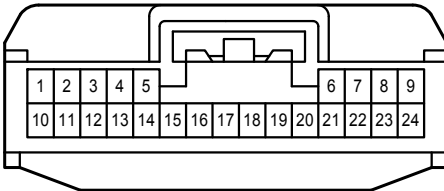
J 58
White



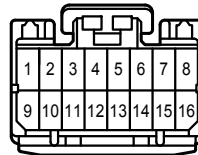
J 75
White



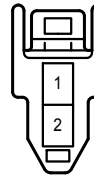
J 76
White



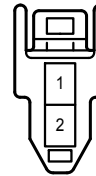
J 77
Gray



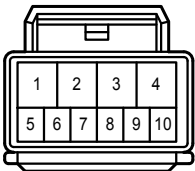
J 81
White



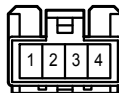
J 84
White



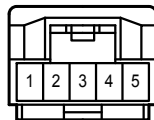
L 8
White



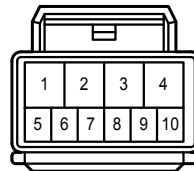
L 9
White



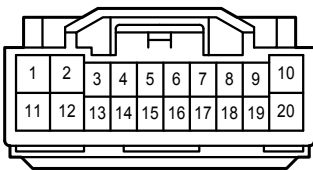
L 19
White



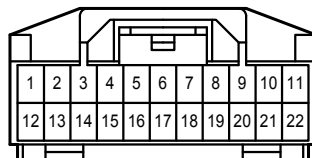
M 2
White



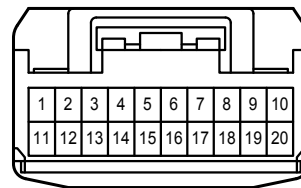
M 7
White



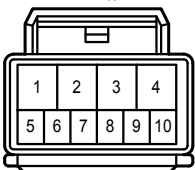
M 14
White



M 23
White



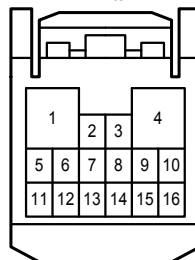
N 8
White



O 8
White



P 1
White



P 9
White



P 16
White



A diagram showing a building-like structure above a 2x22 grid. The grid has two rows of 22 columns each. The columns are numbered 1 through 22. The building structure above the grid has a central section with a smaller section on top, and two side sections. The central section is aligned with columns 4 through 11. The side sections are aligned with columns 1 through 3 and 18 through 22.

[illegible]

Diagram of a 40-pin D-sub connector. The connector is shown from a top-down perspective, with pins numbered 1 through 40. Pins 1-9 are on the left, pins 10-17 are on the right, and pins 18-40 are in the center. The connector has a D-shaped shield and a central locking mechanism.

The diagram shows a 16-point grid with numbered cells. The grid is divided into four quadrants by a vertical line and a horizontal line. The cells are numbered as follows:

1				2		3		4			
5	6	7	8	9	10						
11	12	13	14	15	16						

A diagram of a 5x10 grid. The grid contains 15 numbered cells (1-15) and 5 empty cells. The numbered cells are arranged in three rows of five: the top row contains cells 1-5, the middle row contains cells 6-10, and the bottom row contains cells 11-15. The empty cells are located in the middle row, specifically in the second, fourth, and sixth columns from the left.

A diagram showing a building facade above a 22-column grid. The grid is divided into two rows of 11 columns each. The top row is numbered 1 to 11, and the bottom row is numbered 12 to 22. The building facade has a central entrance and two side wings.

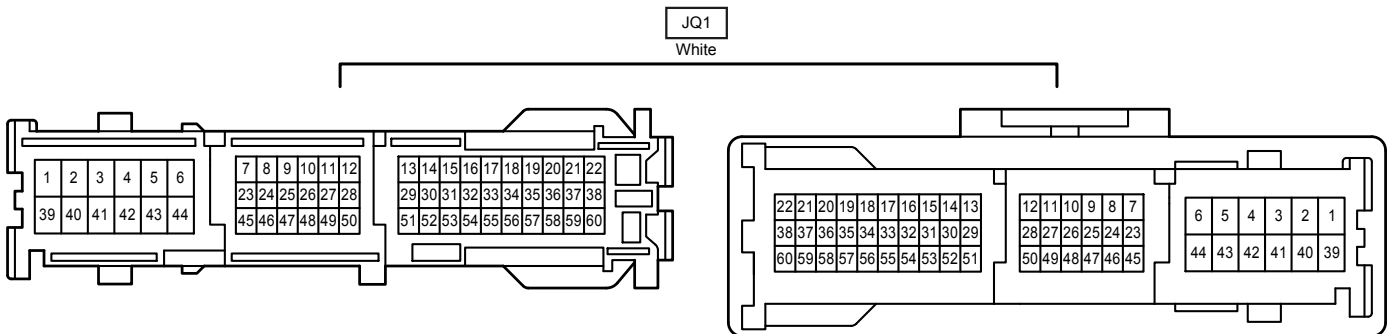
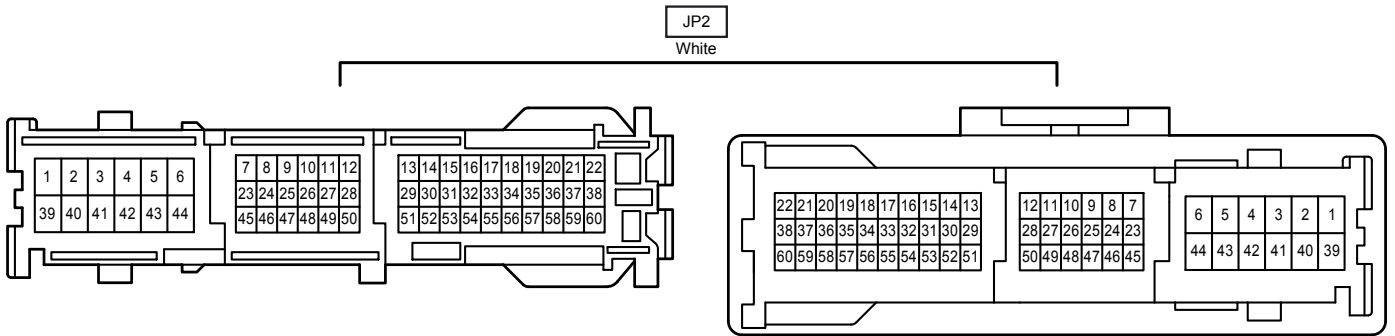
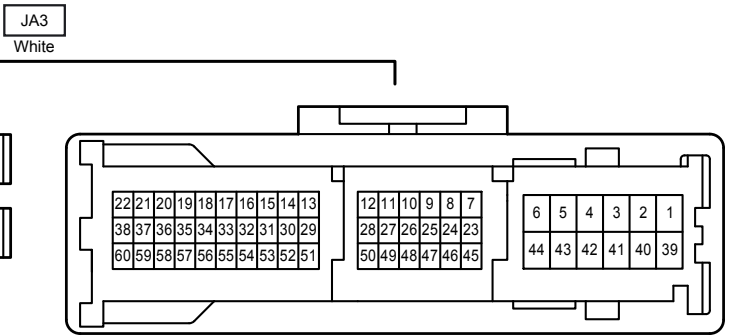
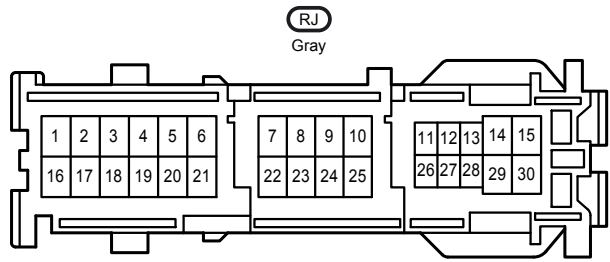
A diagram of a 12-pin D-sub connector. The pins are numbered 1 through 11. Pin 12 is the ground pin, represented by a larger circle at the bottom center of the connector housing.

A top-down diagram of a 28-pin Dual In-Line Package (DIP). The package is rectangular with two rows of pins along the longer sides. The pins are numbered 1 through 28. The numbering starts at the top-left pin (pin 1) and proceeds horizontally to pin 6, then continues on the bottom-left side from pin 15 to pin 20. The right side of the package contains pins 7 through 28, with pin 7 at the top-right and pin 28 at the bottom-right. The diagram shows the physical layout of the package, including the pins and the internal structure.

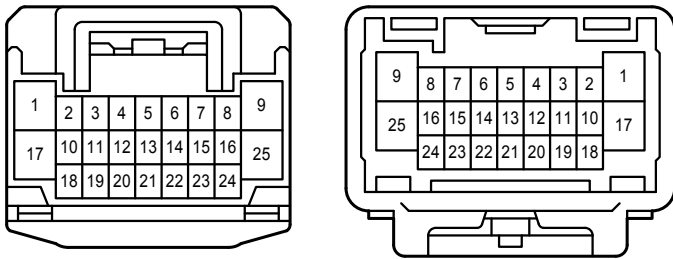
The diagram illustrates a 32-bit bus structure. It consists of three 8-bit data paths (labeled 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32) and a 32-bit address path (labeled 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32). The bus is shown as a horizontal line with multiple segments, each representing an 8-bit data path. The address path is shown as a single line with 32 segments, each representing a bit of the address.

The diagram shows a 30-pin connector layout, likely for a USB or similar interface. The pins are arranged in three rows of 10 pins each. The top row contains pins 1 through 10, the middle row contains pins 11 through 20, and the bottom row contains pins 21 through 30. The pins are numbered 1 through 30, with the numbering starting from the top left and proceeding horizontally across each row.

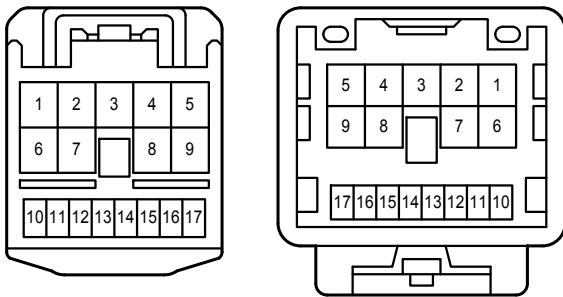
A diagram of a 28-pin DIP package. The pins are numbered 1 through 28. Pins 1-6 are on the left side, pins 7-9 are in the middle, and pins 10-14 are on the right side. Pins 15-20 are on the bottom left, pins 21-23 are in the bottom middle, and pins 24-28 are on the bottom right.



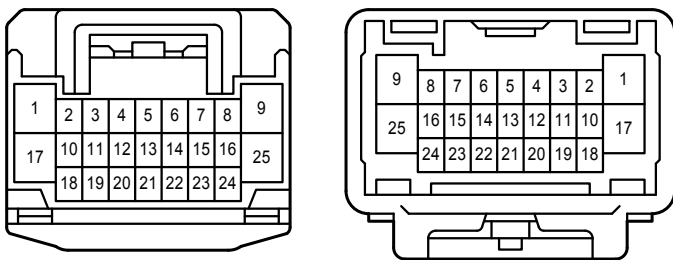
LP1
White



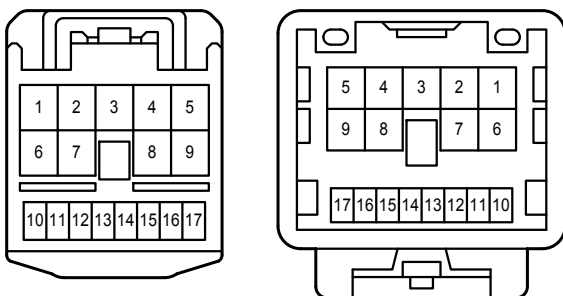
LP2
White



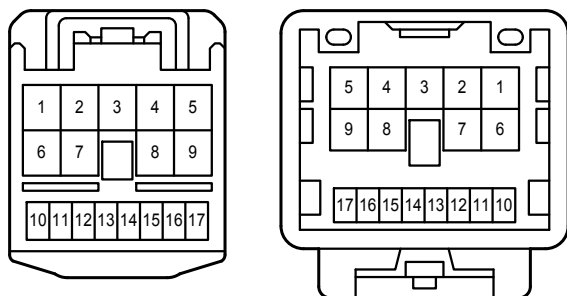
MQ1
White



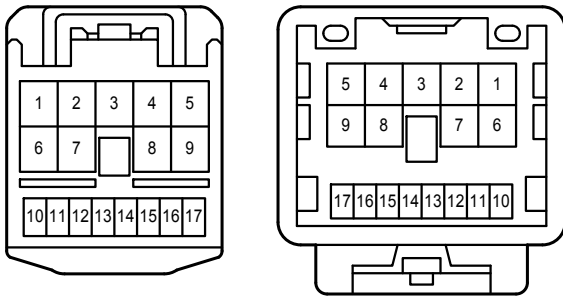
MQ2
White



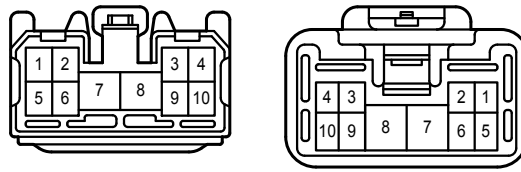
NP1
White



OQ1
White



PQ1
White



PQ2
White

